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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/769,786	02/03/2004	Hak-Ki Choi	6161.0105.US	9242

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EXAMINER	
NGUYEN, JENNIFER T	
ART UNIT	**PAPER NUMBER**
2629	

MAIL DATE	DELIVERY MODE
08/23/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/769,786	CHOI ET AL.	
	Examiner	Art Unit	
	Jennifer T. Nguyen	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 June 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5,7,9,10 and 12* is/are rejected.

7)☒ Claim(s) *2-4, 6, 8, and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office action is responsive to amendment filed on 06/12/07.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 5, 7, 9, 10, and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasa et al. (Patent No.: US 6,937,213) in view of Russell (Patent No.: US 4,029,937).

Regarding claim 1, Iwasa teaches a plasma display panel driving circuit (fig. 13) for generating a ramp pulse for linearly increasing or decreasing a panel capacitor voltage of a plasma display panel (PDP 1, fig. 1), comprising:

a transistor (Q1, fig. 13) in which at least one parasitic capacitance is formed (col. 8, lines 11-15);

a negative feedback element (C1) coupled to the transistor, for performing negative feedback control on a voltage charged in the parasitic capacitance so that the transistor may operate as a constant current source (col. 8, lines 47-53); and

a first capacitor (C3) coupled between a gate and an active node of the transistor (col. 13, lines 40-59).

Iwasa differs from claim 1 in that he does not specifically teach the first capacitor having a temperature characteristic opposite to a temperature characteristic of the negative feedback element.

Russell teaches a capacitor having a temperature characteristic opposite to a temperature characteristic of the negative feedback element (col. 4, lines 2-25). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the capacitor as taught by Russell in the system of Iwasa in order to attain a ramp voltage generating circuit having a highly accurate output signal.

Regarding claim 5, Iwasa teaches the negative feedback element comprises a resistor (R1f, fig. 13) coupled to an output end of the transistor (Q1), and the first capacitor (C3) is coupled between the output end of the transistor and the gate of the transistor (col. 13, lines 28-59).

Regarding claim 7, Iwasa teaches a plasma display panel driving circuit (fig. 14) for generating a ramp pulse for linearly increasing or decreasing a panel capacitor voltage of a plasma display panel (PDP 1, fig. 1), comprising:

a transistor (Q5, fig. 14) having parasitic capacitance formed between a gate and a source thereof (col. 8, lines 11-15);

a first capacitor (C2) coupled between the gate and a drain of the transistor (col. 8, lines 48-54); and

a second capacitor (C4) coupled between the gate and the drain of the transistor (col. 13, lines 40-59).

Iwasa differs from claim 7 in that he does not specifically teach the first capacitor having a temperature characteristic opposite to a temperature characteristic of the first capacitor.

Russell teaches a capacitor having a temperature characteristic opposite to a temperature characteristic of the first capacitor (col. 4, lines 2-25). Therefore, it would have been obvious to

one of ordinary skill in the art at the time the invention was made to incorporate the capacitor as taught by Russell in the system of Iwasa in order to attain a ramp voltage generating circuit having a highly accurate output signal.

Regarding claim 9, Iwasa teaches a plasma display panel driving circuit for generating a ramp pulse for linearly increasing or decreasing a panel capacitor voltage of a plasma display panel (PDP 1, fig. 1), comprising:

a transistor (Q1, fig. 13) having a parasitic capacitance formed between a gate and a source thereof (col. 8, lines 11-15); and

a first capacitor (C1) coupled between the gate and the source of the transistor (col. 8, lines 47-53).

Iwasa differs from claim 9 in that he does not specifically teach the first capacitor having a temperature characteristic opposite to a temperature characteristic of the parasitic capacitance.

Russell teaches a capacitor having a temperature characteristic opposite to a temperature characteristic of the parasitic capacitance (col. 4, lines 2-25). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the capacitor as taught by Russell in the system of Iwasa in order to attain a ramp voltage generating circuit having a highly accurate output signal.

Regarding claim 10, Iwasa teaches a second capacitor (C3) coupled between the gate and a drain of the transistor (col. 13, lines 40-59).

Regarding claim 12, Iwasa teaches a resistor (Rg1, fig. 17) coupled to the source of the transistor (Q1) (col. 17, lines 19-26).

4. Claims 2-4, 6, 8, and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. Applicant's arguments with respect to claims 1-12 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer T. Nguyen whose telephone number is 571-272-7696. The examiner can normally be reached on Mon-Fri: 9:00am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard A. Hjerpe can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer Nguyen
3/17/07

RICHARD HJERPE
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